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| EXAMINER | |
|---|---|
| HO, TU TU V | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

HA

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/605,757 | KINNEY ET AL. | |
| | Examiner | Art Unit | |
| | Tu-Tu Ho | 2818 | |

*-- The MAILING DATE of this communication app ars on th cov r sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *33-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/18/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Oath/Declaration*

1. The oath/declaration filed on 10/23/2003 is acceptable.

### *Claim Rejections § 102 & § 103*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 33** is rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ignatiev et al. U.S. Patent 6,473,332 (the '332 patent).

The '332 patent discloses a method of manufacturing a conductive memory element comprising:

depositing a bottom conductive metal oxide layer ("bottom electrode" 108, column 7, lines 10-15, any of the metal oxides, such as $RuO_2$, in the disclosed list of materials);

depositing onto the bottom conductive metal oxide layer a top conductive metal oxide layer ("top electrode" 112) such that the top conductive metal oxide layer is in electrical communication with the bottom conductive metal oxide layer ("onto" is interpreted broadly as "on" which is interpreted broadly as "above", and this interpretation is applied through the rest of the prosecution);

wherein the top conductive metal oxide layer and the bottom conductive metal oxide layer do not have the same type of either p-type or n-type mobile carriers **(wherein** "wherein the top conductive metal oxide layer and the bottom conductive metal oxide layer do not have the same type of either p-type or n-type mobile carriers" is interpreted broadly as both conductive metal oxides not having (enhanced) n-type or p-type mobile carriers; alternately, since the top conductive metal oxide layer and the bottom conductive metal oxide layer are respectively connected to top and bottom electrodes of sort, which are respectively connected to positive (p-type) and negative (n-type) electrical potential voltage for the device to function, which inherently requires or results in the top conductive metal oxide layer and the bottom conductive metal oxide layer not having the same type of either p-type or n-type mobile **carriers)**; and

wherein the resistance of the conductive memory element can be modified during operation to store information (as the memory element is an electrically variable multi-state resistance computing device (Title) ).

**3.** **Claims 33** is rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Morimoto et al. U.S. Patent Application Publication 2004/0109351 (the '351 publication).

The '351 publication discloses a method of manufacturing a conductive memory element comprising:

depositing a bottom conductive metal oxide layer (221, Figs. 6 and 7, paragraph [0054]);

depositing onto the bottom conductive metal oxide layer a top conductive metal oxide layer (222) such that the top conductive metal oxide layer is in electrical communication with the bottom conductive metal oxide layer;

wherein the top conductive metal oxide layer and the bottom conductive metal oxide layer do not have the same type of either p-type or n-type mobile carriers **(wherein** "wherein the top conductive metal oxide layer and the bottom conductive metal oxide layer do not have the same type of either p-type or n-type mobile carriers" is interpreted broadly as both conductive metal oxides not having (enhanced) n-type or p-type mobile carriers; alternately, since the top conductive metal oxide layer and the bottom conductive metal oxide layer are respectively connected to top and bottom electrodes of sort, which are respectively connected to positive (p-type) and negative (n-type) electrical potential voltage for the device to function, which inherently requires or results in the top conductive metal oxide layer and the bottom conductive metal oxide layer not having the same type of either p-type or n-type mobile **carriers)**; and

wherein the resistance of the conductive memory element can be modified during operation to store information (as the memory element is a phase-change memory (Abstract) ).

**4.** **Claims 33** is rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Zhang et al. U.S. Patent 6,774,054 (the '054 patent).

The '054 patent discloses a method of manufacturing a conductive memory element comprising:

depositing a bottom conductive metal oxide layer (column 2, line 26: "layer of Pr.sub.1-x Ca.sub.x MnO.sub.3 (PCMO) thin film is spin coated on the bottom electrode");

depositing onto the bottom conductive metal oxide layer a top conductive metal oxide layer (column 2, line 46: "The spin-coating process is repeated until the PCMO thin film has a desired thickness" and column 3, line 16: "three spin-coating cycles, resulting in three layers of PCMO thin film") such that the top conductive metal oxide layer is in electrical communication with the bottom conductive metal oxide layer;

wherein the top conductive metal oxide layer and the bottom conductive metal oxide layer do not have the same type of either p-type or n-type mobile carriers **(wherein** "wherein the top conductive metal oxide layer and the bottom conductive metal oxide layer do not have the same type of either p-type or n-type mobile carriers" is interpreted broadly as both conductive metal oxides not having (enhanced) n-type or p-type mobile carriers; alternately, since the top conductive metal oxide layer and the bottom conductive metal oxide layer are respectively connected to top and bottom electrodes of sort, which are respectively connected to positive (p-type) and negative (n-type) electrical potential voltage for the device to function, which inherently requires or results in the top conductive metal oxide layer and the bottom conductive metal oxide layer not having the same type of either p-type or n-type mobile **carriers)**; and

wherein the resistance of the conductive memory element can be modified during operation to store information (column 1, lines 14-27).

**5.** **Claims 33** is rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Hsu et al. U.S. Patent Application Publication 2004/0235247 (the '247 publication).

The '247 publication discloses a method of manufacturing a conductive memory element comprising:

depositing a bottom conductive metal oxide layer (404, Fig. 3, paragraph [0025], such as perovskite metal oxide materials);

depositing onto the bottom conductive metal oxide layer a top conductive metal oxide layer (406) such that the top conductive metal oxide layer is in electrical communication with the bottom conductive metal oxide layer;

wherein the top conductive metal oxide layer and the bottom conductive metal oxide layer do not have the same type of either p-type or n-type mobile carriers **(wherein** "wherein the top conductive metal oxide layer and the bottom conductive metal oxide layer do not have the same type of either p-type or n-type mobile carriers" is interpreted broadly as both conductive metal oxides not having (enhanced) n-type or p-type mobile carriers; alternately, since the top conductive metal oxide layer and the bottom conductive metal oxide layer are respectively connected to top and bottom electrodes 402 and 408, which are respectively connected to positive (p-type) and negative (n-type) electrical potential voltage for the device to function, which inherently requires or inherently results in the top conductive metal oxide layer and the

bottom conductive metal oxide layer not having the same type of either p-type or n-type mobile **carriers)**; and

wherein the resistance of the conductive memory element can be modified during operation to store information (Abstract, "electrical pulse various resistance EPVR)" memory cell structure).

***Election/ Restriction***

6. Applicant's election with traverse of Invention **I, claims 1-32**, in the reply filed on 12/23/2004 is acknowledged. The traversal is on the ground(s) that (1) linking claim 33 should not be associated with a group since such claims must be examined with any of the linked inventions that might be elected and (2) the process in claim 33 of Invention II can not be used to make a product different from the product of Invention I, for example the product of claim 27. This is not found persuasive because (1) while it is true that a linking claim must be examined with any of the linked inventions that might be elected, it is not required to not be associated with a group. Furthermore, the linking claim is to be examined only to the extent necessary to determine if the linking claim is unpatentable. If the linking claim is unpatentable, restriction is proper (MPEP 806.05(e) ); and (2) as stated in the example in the restriction requirement, the process in claim 33 of Invention II could be used to make a floating-gate-transistor memory cell. Claim 1 or claim 27 of Invention I requires a first electrode and a second electrode, and requires a first conductive metal oxide layer stacked upon and in electrical communication with the first electrode. By contrast, claim 33 of Invention II does not require any of the first and second electrodes. Claim 33 requires only "depositing onto the bottom conductive metal oxide layer a

top conductive metal oxide layer such that the top conductive metal oxide layer is in electrical communication with the bottom conductive metal oxide layer", without the additional first and second electrodes as required in claim 1 or claim 27. As such, the bottom conductive metal oxide layer and the top conductive metal oxide layer could be used as contact or electrode layers for the floating gate and/or the control gate of the floating-gate-transistor memory cell.

Since the linking claim is unpatentable, as noted above, the requirement is still deemed proper and is therefore made FINAL.

7. **Claims 33-45** are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **with** traverse, as noted above.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
>
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
>
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. **Claims 1, 5-6, 25, and 27-29** are rejected under 35 U.S.C. 102(e) as being anticipated by the '054 patent.

The '054 patent discloses in Fig. 3 and respective portions of the specification a conductive memory device as claimed.

Referring to **claim 27** and using the same reference characters, citations, and interpretations as detailed above for claim 33 where applicable, the '054 patent discloses a conductive memory device capable of storing information comprising:

a first electrode (not shown in the figure but disclosed in column 2, line 25-27, as bottom electrode);

a first conductive metal oxide layer stacked upon and in electrical communication with the first electrode;

a second conductive metal oxide layer stacked upon and in electrical communication with the first conductive metal oxide layer; and

a second electrode ("top electrode", column 2, line 59) stacked upon and in electrical communication with the second conductive metal oxide layer; wherein

the conductive memory element has a resistivity that is indicative of the information stored therein.

Referring to **claim 1** and using the same reference characters, citations, and interpretations as detailed above for claims 33 and 27 where applicable, the '054 patent discloses a conductive memory device capable of storing information comprising:

a first electrode;

a first conductive metal oxide layer stacked upon and in electrical communication with the first electrode;

a second conductive metal oxide layer stacked upon and in electrical communication with the first

conductive metal oxide layer;

a third conductive metal oxide layer stacked upon and in electrical communication with the second conductive metal oxide layer; and

a second electrode stacked upon and in electrical communication with the third conductive metal oxide layer; wherein the conductive memory element has a resistance that is indicative of the information stored therein.

Referring to **claims 5 and 28**, the '054 patent further discloses that the resistance of the conductive memory element may be increased by applying a first voltage having a first polarity across the first and second electrodes and decreased by applying a second voltage having a second polarity across the conductive memory element (column 1, lines 14-27).

Referring to **claims 6 and 29**, since the '054 patent discloses that the "resistor may be reversibly programmed to a high or a low resistance state by unipolar electrical pulses having different pulse widths" (column 1, lines 14-27), it follows that an initialization pulse across the first and second electrodes has no effect on establishing which polarity is needed to increase the resistance of the conductive memory element.

Referring to **claim 25**, the '054 patent further discloses that the conductive memory element is rewriteable (column 1, lines 14-27).

**9.** **Claims 27-29** are rejected under 35 U.S.C. 102(e) as being anticipated by the '247 publication.

The '247 publication discloses in Fig. 3 and respective portions of the specification a conductive memory device as claimed.

Referring to **claim 27** and using the same reference characters, citations, and interpretations as detailed above for claim 33 where applicable, the '247 publication discloses a conductive memory device capable of storing information comprising:

a first electrode (402);

a first conductive metal oxide layer (404) stacked upon and in electrical communication with the first electrode;

a second conductive metal oxide layer (406) stacked upon and in electrical communication with the first conductive metal oxide layer; and

a second electrode (408) stacked upon and in electrical communication with the second conductive metal oxide layer; wherein

the conductive memory element has a resistivity that is indicative of the information stored therein.

Referring to **claim 28**, the '247 publication further discloses that the resistance of the conductive memory element may be increased by applying a first voltage having a first polarity across the first and second electrodes and decreased by applying a second voltage having a second polarity across the conductive memory element (paragraphs [0027] and [0028]).

Referring to **claim 29**, since the '247 publication discloses that the either a positive or a negative pulse (a positive or a negative pulsed electric filed) can increase the resistance of the conductive memory element (can increase or decrease the resistance of the first conductive metal oxide layer 404 (paragraph [0027]), which constitutes the conductive memory element), it

follows that an initialization pulse across the first and second electrodes has no effect on establishing which polarity is needed to increase the resistance of the conductive memory element.

Referring to **claim 30**, the '247 publication further discloses that the resistivity that is indicative of the information stored occurs in the first conductive metal oxide layer (404, paragraph [0027]).

*Claim Rejections § 102 & § 103*

**10. Claims 2, 21-24, 30, and 32** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over the '054 patent.

Referring to **claim 2**, it appears that the '054 patent's first, second and third conductive metal oxide layers, which constitutes the well-crystallized PCMO thin film, are substantially compatible for them to function as a "a well-crystallized PCMO thin film having bipolar electrical pulse switching properties for use in RRAM applications" (column 1, lines 60-65).

Referring to **claims 21-24**, since the '054 patent discloses that the object of its invention is to form a well-crystallized PCMO thin film having bipolar electrical pulse switching properties for use in RRAM applications, as noted above for claim 2, it appears that the reference discloses crystalline characteristics, lattice parameters, and compositional similarity as claimed.

Referring to **claims 30 and 32**, since the '054 patent is silent about the specific layer of the three layers to store information, it appears that the resistivity that is indicative of the information stored could occur in the first conductive metal oxide layer as recited in claim 30 or could occur in the second conductive metal oxide layer as recited in claim 32.

**11.** **Claim 32** is rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over the '247 publication.

As noted above for claim 30, the '247 publication discloses that the resistivity that is indicative of the information stored occurs in the first conductive metal oxide layer (404). The reference fails to disclose that the resistivity that is indicative of the information stored occurs in the second conductive metal oxide layer (406) as recited in claim 32. Nevertheless, the reference anticipates the claim if one interprets first-second and up-down relatively. Specifically, since the claim requires only the two electrodes sandwiching the two conductive metal oxide layers, any of the two could be labeled first or second. Alternately, since the criticality of the relative positions of the two electrodes or the criticality of the relative positions of the two conductive metal oxide layers has not been established, moving them around would not effect the outcome of the resistive memory cell and therefore would have been obvious.

***Claim Rejections - 35 USC § 103***

**12.** **Claims 17-20** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '054 patent.

Referring to the claimed thicknesses of the various layers (first, second, and third conductive metal oxide layers) of **claims 17-20**, which thicknesses ranging from 10 to 1000 angstroms, although the '054 patent is silent about a particular thickness for the various layers, the reference teaches, as detailed above for claims 1, 27, and 33, spin-coating a first layer, a second layer, a third layer, and repeating spin-coating until the final PCMO film, which

constitutes the resistive memory element, has a desired thickness (column 2, lines 45-50). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's first, second, and third conductive metal oxide layers so that they have various thickness as claimed so that their combined thickness has a desired thickness. See, for example, Kaneko et al. U.S. Patent 5,666,217 for a disclosure that thin-film thickness as thin as 30 Angstroms could be formed each cycle.

**13.** **Claim 31** is rejected under 35 U.S.C. §103(a) as being unpatentable over the '247 publication in view of knowledge in the art as disclosed by Noguchi et al. U.S. Patent 6,323,525 (the '525 patent).

The '247 publication discloses a conductive memory device as claimed and as detailed above for claim 27 including the first and second conductive metal oxide layers, but fails to disclose that either the first or second conductive metal oxide layer is strontium zirconate. The reference further fails to disclose that either the first or second conductive metal oxide layer is doped as n-type semiconductor and the remaining of the first or second conductive metal oxide layer is doped as a p-type semiconductor. However, conductive metal oxide strontium zirconate, similarly to perovskite metal oxide materials as disclosed by the reference (paragraph [0025]), is a conductive perovskite metal oxide material, and therefore the use of conductive metal oxide strontium zirconate for a conductive metal oxide, instead of a conductive perovskite metal oxide material would have been obvious to one of ordinary skill in the art. See, for example, Pique et al. U.S. Patent 6,074,990, column 5, for a disclosure that strontium zirconate (SZO) is used as a conductive metal oxide.

As noted, the reference also fails to disclose that either the first or second conductive metal oxide layer is doped as n-type semiconductor and the remaining of the first or second conductive metal oxide layer is doped as a p-type semiconductor. In other words, the reference fails to discloses that either the first or second conductive metal oxide layer has (more) n-type mobile carriers, which effects the conductivity (and thus the resistivity) of the layer with respect to a particular polarity of the applied electrical voltage as is known in the art, and the remaining of the first or second conductive metal oxide layer has (more) p-type mobile carriers, which effects the conductivity (and thus the resistivity) of the layer with respect to a particular polarity of the applied electrical voltage as is known in the art. In shorter words, the reference fails to disclose that the first and second conductive metal oxide layers are asymmetric in term of mobile carriers with respect to a particular polarity of the applied electrical voltage. However, the reference teaches that the first and second conductive metal oxide layers are asymmetric in term of crystalline characteristics, which effect the conductivity (and thus the resistivity) of the layers with respect to an applied electrical voltage as is known in the art. What is missing from the reference as far as the claim is concerned are the respective dopants (n-type and p-type doped). Nevertheless, the use of dopants to effect electrical conductivity is known in the semiconductor art, for example, disclosed by the '525 patent, which, in disclosing a semiconductor device, discloses that a polysilicon, metal, or conductive metal oxide layer when doped with n-type or p-type (phosphorus, arsenic, or boron ion-implantation) effects the resistivity (and thus conductivity) of the layer (column 21, last full paragraph).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's first or second conductive metal oxide layer with

doped n-type semiconductor and the remaining of the first or second conductive metal oxide layer with doped p-type semiconductor. One would have been motivated to make such a change because, as is known in the art, n-type or p-type dopant effect the resistivity with respect to a particular polarity of the applied electrical voltage.

**14.** **Claims 3-4, 7-16, 26, and 31** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '054 patent in view of knowledge in the art as disclosed by the '525 patent.

The '054 patent discloses a conductive memory device as claimed and as detailed above for claims 1 and 27 including the first, second, and third conductive metal oxide layers as recited in claim 1 or including the first and second conductive metal oxide layers as recited in claim 27, but fails to disclose that either the first or third (or second as recited in claim 27) conductive metal oxide layer is strontium zirconate or other conductive metal oxide materials as claimed in claims 9-16 and 31. The reference further fails to disclose that the first conductive metal oxide layer is n-type or p-type and the third conductive metal oxide layer is of opposite type as recited in claim 3; or that the first and third conductive layers are both of the same n-type or p-type, with different concentrations of mobile carriers as cited in claims 4 and 15-16 or at least one of the conductive metal oxide layers includes up to 10% dopant as recited in claim 26; or that either the first or second conductive metal oxide layer is doped as n-type semiconductor and the remaining of the first or second conductive metal oxide layer is doped as a p-type semiconductor as recited in claim 31;. However, conductive metal oxide materials such as strontium zirconate, similarly to perovskite metal oxide materials as disclosed by the reference (column 2,lines 20-27), is a conductive perovskite metal oxide material, and therefore the use of conductive metal oxide

strontium zirconate for a conductive metal oxide, instead of a conductive perovskite metal oxide material would have been obvious to one of ordinary skill in the art. See, for example, Pique et al. U.S. Patent 6,074,990, column 5, for a disclosure that strontium zirconate (SZO) is used as a conductive metal oxide.

As noted, the reference also fails to disclose that the first conductive metal oxide layer is n-type or p-type and the third conductive metal oxide layer is of opposite type as recited in claim 3; or that the first and third conductive layers are both of the same n-type or p-type, with different concentrations of mobile carriers as cited in claims 4 and 15-16 or at least one of the conductive metal oxide layers includes up to 10% dopant as recited in claim 26; or that either the first or second conductive metal oxide layer is doped as n-type semiconductor and the remaining of the first or second conductive metal oxide layer is doped as a p-type semiconductor as recited in claim 31. In other words, the reference fails to disclose using various dopants and materials to effect conductivity and polarity of the respective conductive metal oxide layers. Nevertheless, as noted above in paragraph numbered 13, the use of dopants, and thus materials, to effect conductivity and polarity of the respective conductive metal oxide layers are known in the art and therefore would have been obvious to one of ordinary skill in the art the time the invention was made.

## *Conclusion*

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
January 28, 2005